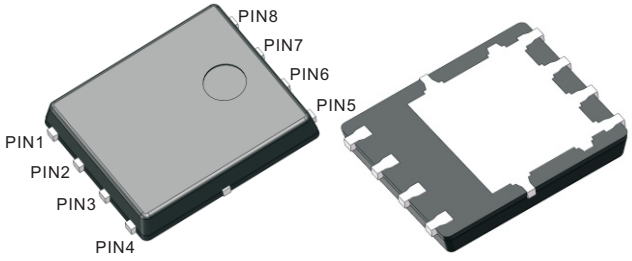
145A 40V N-CHANNEL POWER MOSFET

PDFN5060-8L(Prefix :L)

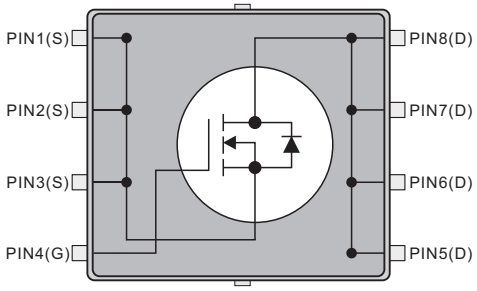


Description

This model is an n-channel enhanced MOS power field effect transistor manufactured by silicon epitaxial process. This model has excellent switching characteristics, extremely low on impedance, low gate charge and other characteristics.

Features

- SGT technology
- Moisture sensitivity level 1
- $R_{DS(ON)}$ <2.8mΩ @ V_{GS}=10V, I_D=20A
- Extremely low on impedance
- Low gate charge
- Superior switching characteristics
- 100% Avalanche tested
- 100% △V_{DS} tested



S:Source
G:Gate
D:Drain

RoHS COMPLIANT

Mechanical data

- Case: PDFN5060-8L
- Approx. Weight:0.093g (0.0032oz)
- RoHS compliant
- Case Material: “Green” molding compound, UL flammability classification 94V-0,“Halogen-free”.

Absolute Maximum Ratings (Ta=25°C, Unless Otherwise Specified)

Parameter	Symbols	Ratings	Units
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current V_{GS}=10V,Tc=25℃	I_D	145	A
Pulsed Drain Current Tc=25 °C	I_{DM}	581	A
Avalanche energy, single pulse(Note1)	E_{AS}	216	mJ
Power dissipation Tc=25 °C	P_{tot}	100	W
Operating junction and storage temperature	T_j,T_{stg}	-55 ~ +175	°C

Thermal Characteristics

Parameter	Symbols	Ratings	Units
Device on PCB cooling area (Note2)	R_{thJA}	60	°C/W
Thermal resistance, junction - case	R_{thJC}	1.8	°C/W

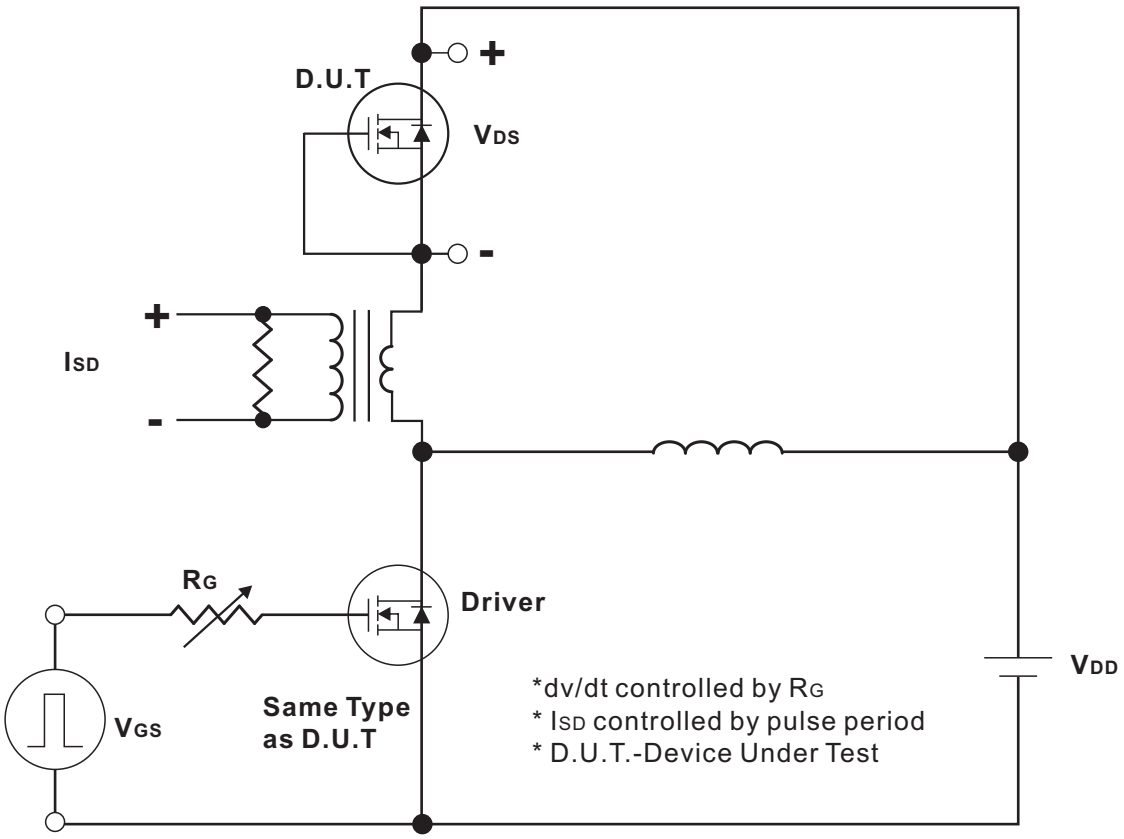
NOTE:
1.L=0.5mH, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
2.Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR-4 with 6 cm2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Electrical Characteristics (Ta=25°C, Unless Otherwise Specified)

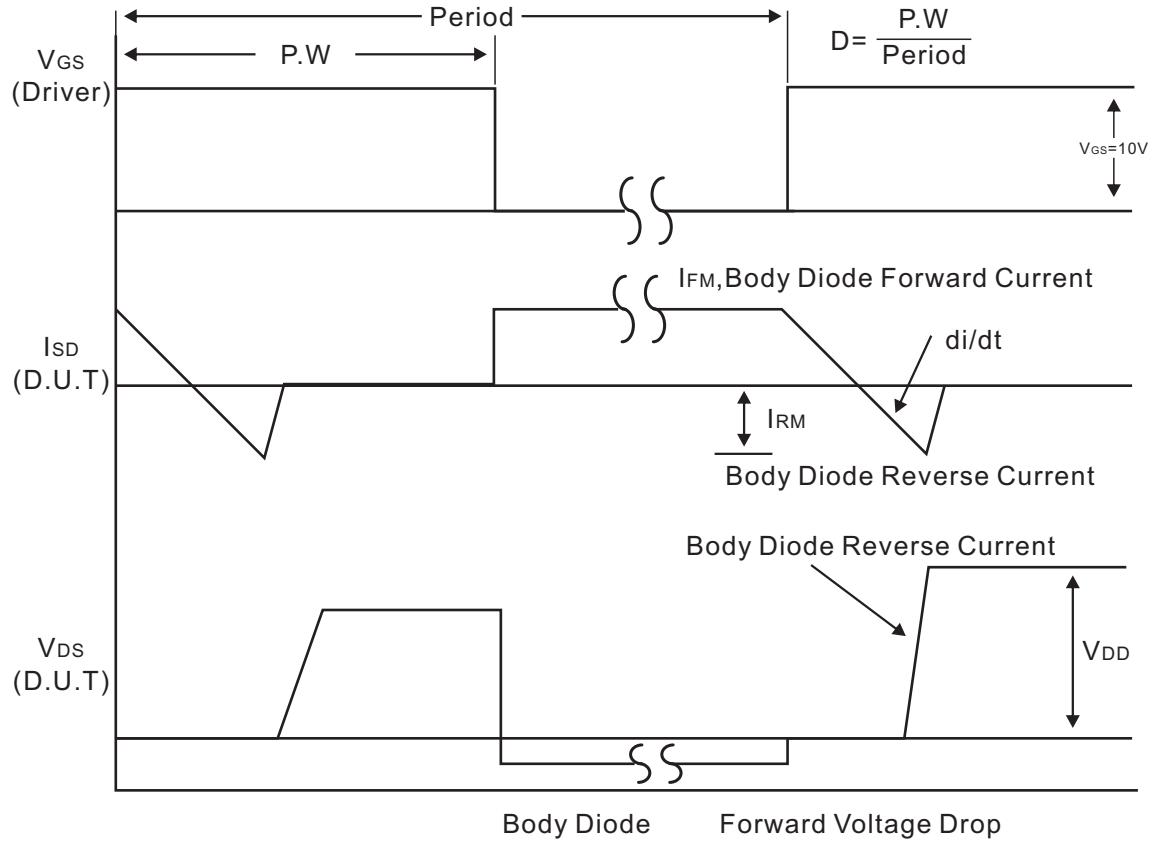
Parameter	Symbols	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	40			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=20A		2.2	2.8	mΩ
Transconductance	g_{fs}	V_{DS}=5V,I_D=20A		30		S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}=20V,		2086		pF
Output Capacitance	C_{OSS}	V_{GS}=0V,		1150		pF
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz		60		pF
Gate Resistance	Rg			1.4		Ω
Switching Characteristics						
Total Gate Charge (Note 1)	Q_G	V_{DS}=20V,V_{GS}=10V,		28		nC
Gate-Source Charge	Q_{GS}	I_D=20A(NOTE1,2)		9.2		nC
Gate-Drain Charge	Q_{GD}			5.3		nC
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	V_{DS}=20V,V_{GS}=10V,		63		ns
Turn-On Rise Time	t_R	R_G=6Ω,I_D=20A		14.8		ns
Turn-Off Delay Time	$t_{D(OFF)}$	(NOTE1,2)		31		ns
Turn-Off Fall Time	t_F			87		ns
Drain-source Diode Characteristics And Maximum Ratings Description						
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	I_{SD}=1A,V_{GS}=0V			1.0	V
Diode continuous forward current	I_S	Tc=25°C			100	A
Reverse Recovery time	trr	V_{GS}=0V,I_{SD}=20A di/dt=100A/us		39		nS
Reverse Recovery Charge	Qrr			29		nC

Notes:
1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

Test Circuits and waveforms

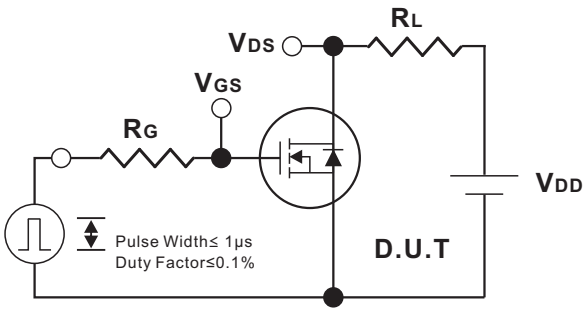


Peak Diode Recovery dv/dt Test Circuit

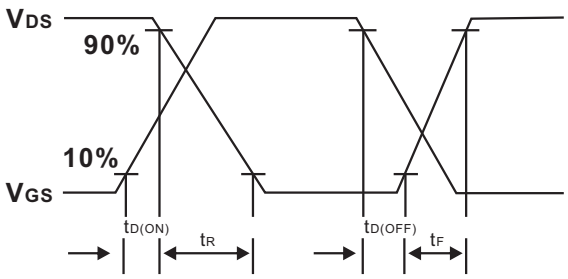


Peak Diode Recovery dv/dt Waveforms

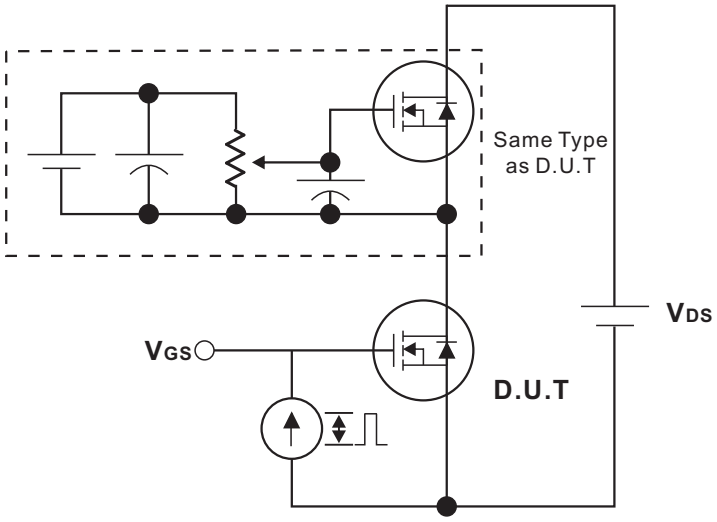
Test Circuits and waveforms



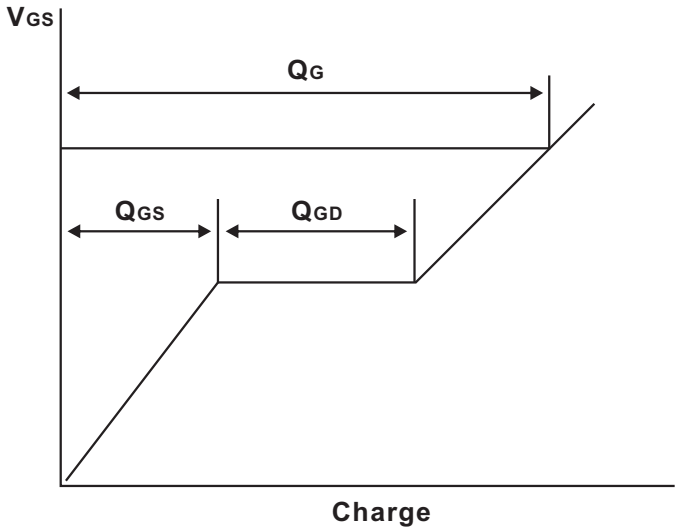
Switching Test Circuit



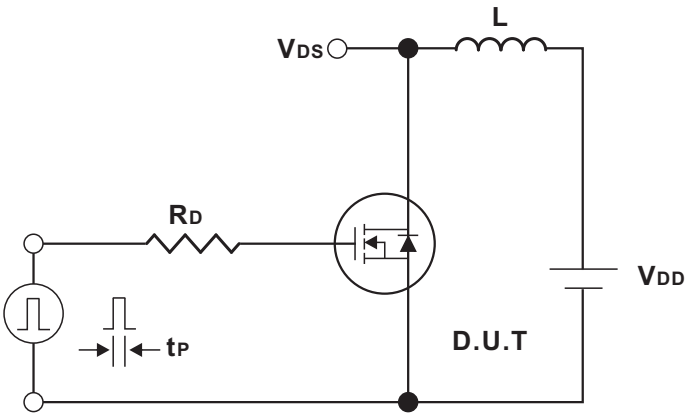
Switching Waveforms



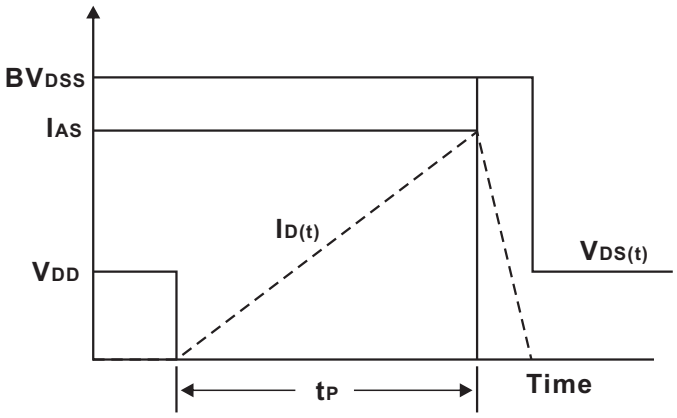
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Typical Characteristics

Fig.1 Output characteristics

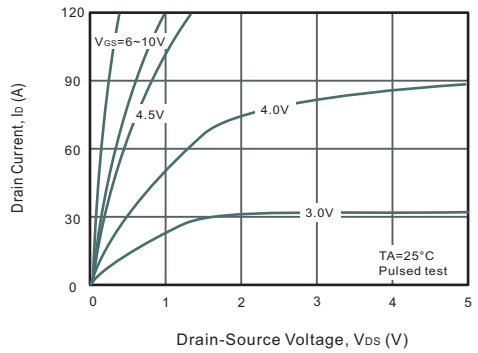


Fig.2 Power Dissipation

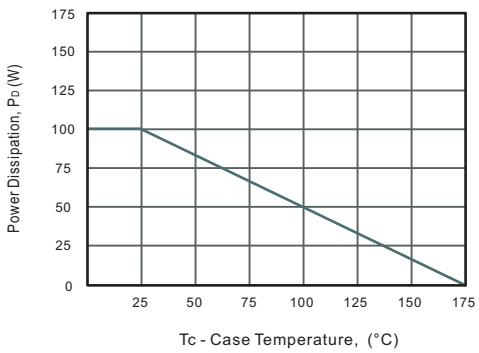


Fig.3 Drain Current Derating

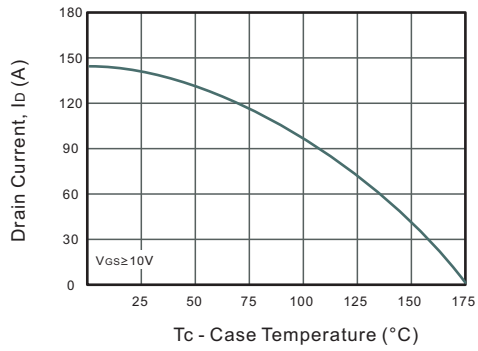


Fig.4 Drain-Source On-Resistance vs. Drain Current

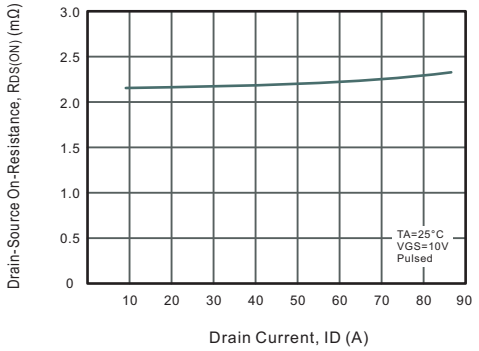


Fig.5 Gate Threshold Voltage vs. Junction Temperature

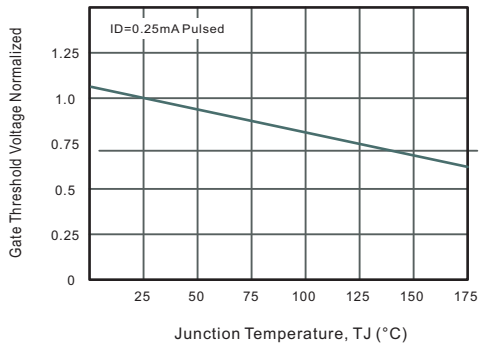


Fig.6 Body-diode Forward Characteristics

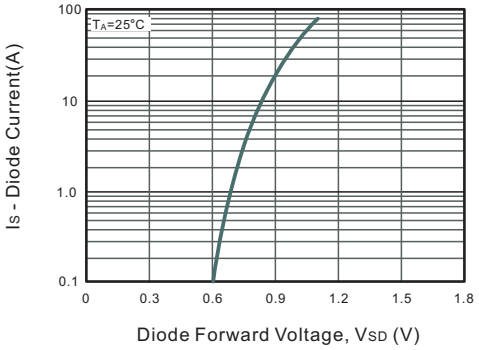


Fig.7 Drain-Source On-Resistance vs. Junction Temperature

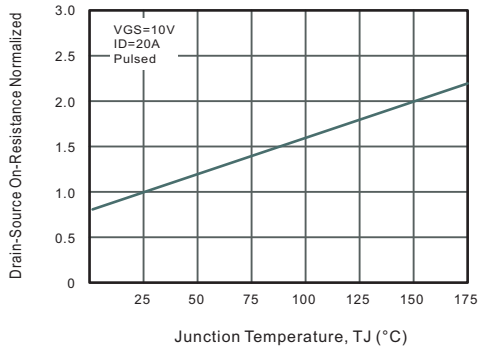
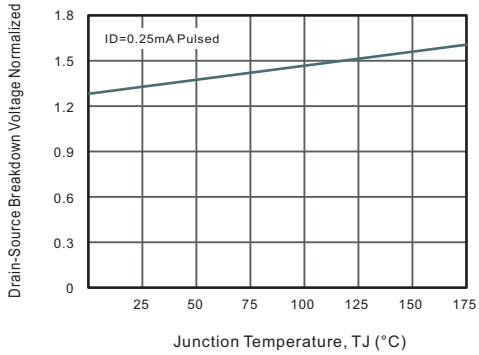


Fig.8 Breakdown Voltage vs. Junction Temperature



Typical Characteristics

Fig.9 Capacitance Characteristics

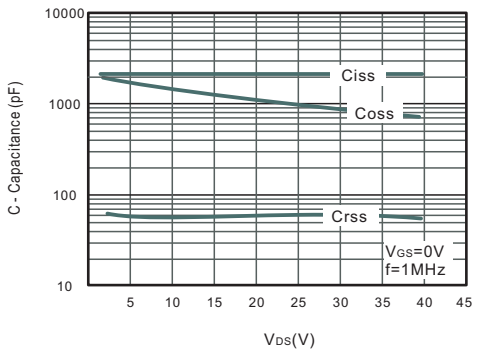


Fig.10 Gate Charge Characteristics

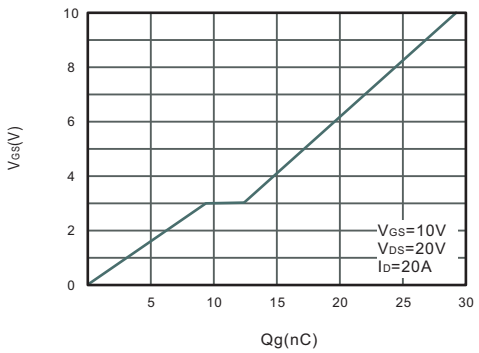


Fig.11 Safe Operating Area

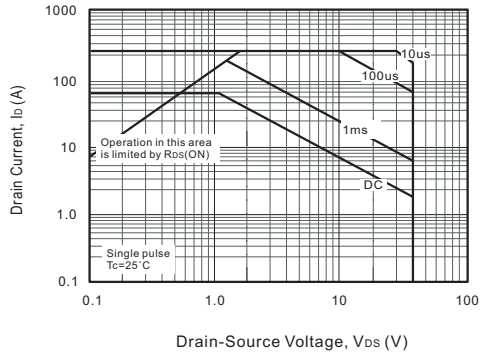
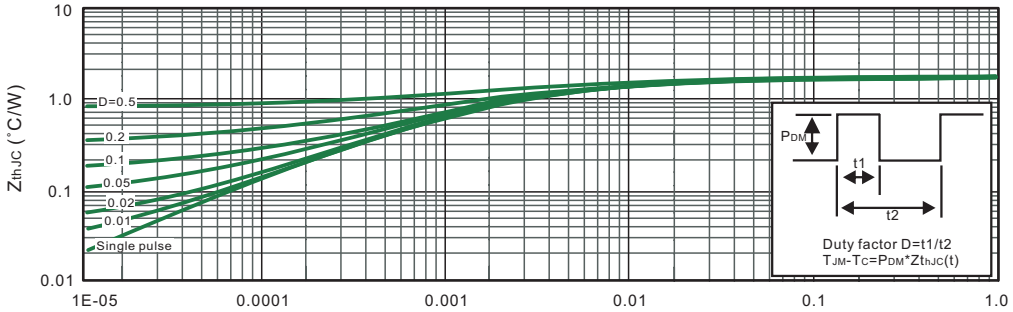
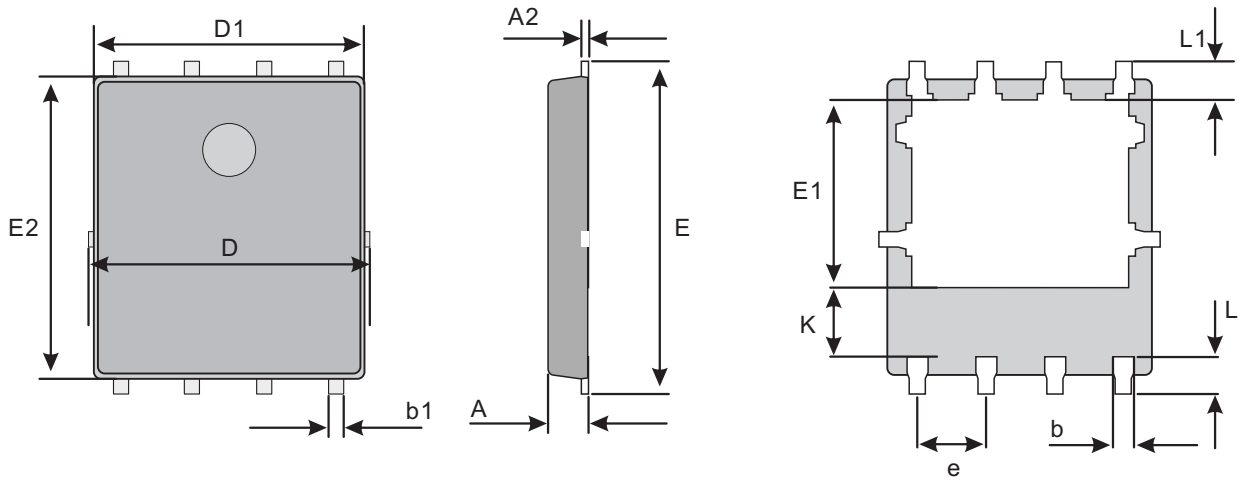


Fig.12 Max. Transient Thermal Impedance



Package Outline
Plastic surface mounted package;8 leads **PDFN5060-8L**



Mechanical data

UNIT		A	A2	b	b1	D	D1	E	E1	E2	e	K	L	L1
mm	max	1.1	0.304	0.4 ref.	0.4	5.3	5.24	6.35	3.675	6.09	1.27 typ.	1.29 typ.	0.785	0.7 typ.
	typ	1.0	0.254		0.3	5.15	5.04	6.15	3.475	5.89			0.685	
	min	0.9	0.204		0.2	5.0	4.84	5.95	3.275	5.69			0.585	
mil	max	43	12	16 ref.	16	209	206	250	145	240	50 typ.	51 typ.	31	28 typ.
	typ	39	10		12	203	198	242	137	232			27	
	min	35	8		8	197	191	234	129	224			23	

Marking

Type number	Marking code
L2R2NS40HR	L2R2NS40HR

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